Attorney Docket: 012.P10008

REMARKS

Claims 2-5 and 7-49 are pending in the above-referenced patent application. In this response, no claims have been added, cancelled or amended.

The above-referenced patent application has been reviewed in light of the Office Action, dated August 19th, 2005, in which: claims 2-3, 5, 7-9, 17-18, 20-24, 44-46 and 49 are rejected under 35 U.S.C 102(e) as being anticipated by Grisamore (U.S. Patent No. 6,535,901, hereinafter "Grisamore"); claims 4, 10-12, 19 , 25-27 and 47-48 are rejected under 35 U.S.C 103(a) as being obvious over Grisamore and in view of Chang et al. (Hardware-efficient implementations for discrete function transforms using LUT-based FPGAs, Nov. 1999, IEEE Computers and Digital Techniques, pages 309-315, hereinafter "Chang"); claims 13-16 and 28-31 are rejected under 35 U.S.C 103(a) as being obvious over Grisamore in view of Chang, and further in view of Fang et al. ("A hierarchical function structuring and partitioning approach for multiple-FPGA implementations, Oct. 1997, IEEE Computer-Aided Design of Integrated Circuits and Systems, pages 1188-1195, hereinafter "Fang"); claims 32, 36-38 and 42-43 are rejected under 35 U.S.C 103(a) and being obvious over Grisamore in view of Greenberger (U.S. Patent No. 6,411,979, hereinafter "Greenberger"); claims 33-35 are rejected under 35 U.S.C 103(a) and being obvious over Grisamore in view of Greenberger, in view of Chang; claims 39-41 are rejected under 35 U.S.C 103(a) and being obvious over Grisamore in view of Greenberger, in view of Chang, and in further view of Fang. Reconsideration of the above-referenced patent application in view of the following remarks is respectfully requested.

Assignee respectfully submits that Grisamore does not disclose each and every element of the rejected claims, and, therefore, a prima facie case under 35 U.S.C. 102(e) has not been established. For example, Grisamore does not disclose one or more full-adders and associated registers, half-adders and associated registers, and single registers to produce intermediate summation results by combining the input terms according to a pipelined reduction pattern. Grisamore clearly describes passing partial products to an adder to perform adding functions, and passing and subsequently retrieving carry terms from a memory device [Col. 2:63-3:8.], rather than utilizing an apparatus having associated registers. Assignee is unable to find any description throughout Grisamore of registers implemented in a manner as recited in the rejected claims. It is respectfully requested that the

Examiner cite the portion of Grisamore that describes registers implemented outside a memory device, and implemented as one or more full-adders and associated registers, half-adders and associated registers, and single registers, as recited in the rejected claims.

In the Response to Arguments, the Examiner states, "As indicated in col. 1 lines 32-41, col. 3 lines 19-27 and col. 6 lines 60-68 [of Grisamore], during pipelining there must be associated registers to store the partial results of each adder before loading into the next stage of pipeline wherein the associated registers and single registers are registers at optimal points in the array multiplier." However, Assignee is unable to locate "associated registers" as described by the Examiner, and it is respectfully requested that the Examiner explicitly cite the teaching of using "associated registers" from Grisamore. The cited portion of Grisamore, referenced from the Background section, describe registers implemented in an array multiplier, and does not show or describe registers implemented in "a multi-stage series of Boolean function generators", as claimed in claim 2. Therefore, it is respectfully submitted that Grisamore does not show or describe "a multi-stage series of Boolean function generators coupled with the inputs to implement one or more full-adders and associated registers, half-adders and associated registers, and single registers" as recited in claim 2, and, therefore, a prima facie case under 35 U.S.C. 102(e) has not been established.

Therefore, Assignee respectfully submits that because Grisamore does not disclose each and every element of the rejected claims, a prima facie case under 35 U.S.C. 102(e) has not been established, and claim 2 is in a condition for allowance. Claim 17 is in a condition for allowance for at least the same reasons as claim 2. Additionally, claims 3, 5, 7-9, 18, 20-24 and 44-46 and 49 either depend from or include similar limitations as claims 2 or 17, and these claims are in a condition for allowance for at least similar reasons as claims 2 and 17.

The Examiner has rejected claims 4, 10-12, 19 25-27 and 47-48 under 35 U.S.C 103(a) as being obvious over Grisamore and in view of Chang, claims 13-16 and 28-31 under 35 U.S.C 103(a) as being obvious over Grisamore in view of Chang, and further in view of Fang, claims 32, 36-38 and 42-43 under 35 U.S.C 103(a) as being obvious over Grisamore in view of Greenberger, claims 33-35 under 35 U.S.C 103(a) and being obvious over Grisamore in view of Greenberger, in view of Chang,

and claims 39-41 under 35 U.S.C 103(a) and being obvious over Grisamore in view of Greenberger, in view of Chang, and in further view of Fang.

It is respectfully submitted that Grisamore whether viewed alone or in combination with Chang, Fang and/or Greenberger, does not contain all of the elements of the rejected claims. However, Assignee does not by this argument accept that the combination is proper; rather, while Assignee asserts that the combination is improper, Assignee further asserts that even if the combination were proper, the combination would still fail to provide all the elements of the rejected claims.

Assignee begins with claim 4, rejected under 35 U.S.C 103(a) as being obvious over Grisamore and in view of Chang. The Examiner already concedes that Grisamore is lacking one or more elements of the rejected claims. For example, the Examiner states: "Grisamore does not disclose the Boolean function generator compris[ing] four-input look-up tables (LUTs) to implement Boolean logic functions. However, Chang et al. disclose[s] in Figure 1(a) Boolean function generator compris[ing] four-input look-up tables (LUTs) to implement Boolean logic functions." However, even if the successful combination of Grisamore and Chang were made, although, as stated previously, Assignee has serious doubts concerning the ability to do so, the resultant combination or any of the other alleged combinations would still not recite the elements of claim 4. As just an example, Chang is directed generally toward LUT based FPGAs, and does not show or describe a multi-stage series of Boolean function generators coupled with the inputs to implement one or more full-adders and associated registers, half-adders and associated registers, and single registers to produce intermediate summation results. Additionally, as noted above, Grisamore does not cure this deficiency, and, therefore, any resultant combination of Grisamore and Chang would not produce the elements of claim 4.

It is respectfully submitted, therefore, that at least one element of claim 4 is absent from the cited art, and any alleged combination would still not result in a combination having each element of the rejected claim. Therefore, at least one prong of the three-prong test for obviousness has not been satisfied, and a prima facie case of obviousness under section 103 of the patent statute has not been made. It is, therefore, respectfully submitted that claim 4 is in condition for allowance.

Claims 10-12, 19, 25-27 and 47-48 distinguish from the cited art at least on the same basis. It is therefore respectfully requested that the Examiner withdraw his rejection of these claims.

The Examiner has rejected claims 13-16 and 28-31 under 35 U.S.C 103(a) as being obvious over Grisamore in view of Chang, and further in view of Fang. This rejection by the Examiner is also respectfully traversed. The Examiner already concedes that Grisamore is lacking one or more elements of the rejected claims. For example, the Examiner states: "Grisamore does not disclose in Figures 1, 4-5, and 7 a controller or a logic module dynamically structures the atomic elements of the dedicated logic device. However, Fang et al. disclose in Figure 3 a controller or a logic control module dynamically ... structures the atomic elements of the dedicated logic device." However, even if the successful combination of Grisamore, Chang and Fang were made, although, as stated previously, Assignee has serious doubts concerning the ability to do so, the resultant combination or any of the other alleged combinations would still not recite the elements of the rejected claims. Fang is directed toward structuring and partitioning of FPGA implementations. The cited passage recites hierarchical structuring of an FPGA implementation, and does not provide the deficiencies of Grisamore, noted above. For example, neither Grisamore, Chang nor Fang recite a multi-stage series of Boolean function generators coupled with the inputs to implement one or more full-adders and associated registers, half-adders and associated registers, and single registers to produce intermediate summation results. As stated previously, the cited portion of Grisamore referencing registers is referring to an array multiplier, and does not show or describe registers implemented in "a multi-stage series of Boolean function generators". Assignee again respectfully requests that the Examiner explicitly cite the portion of Grisamore that teaches the use of one or more full-adders and associated registers, half-adders and associated registers, and single registers.

It is respectfully submitted that because at least one element of claims 13-16 and 28-31 are absent from the cited art, any alleged combination would still not result in a combination having each element of the rejected claim. It is, therefore, respectfully submitted that claims 13-16 and 28-31 are in condition for allowance.

The Examiner has rejected claims 32, 36-38, and 42-43 under 35 U.S.C 103(a) as being obvious over Grisamore in view of Greenburger, claims 33-35 under 35 U.S.C 103(a) as being obvious

over Grisamore in view of Greenburger, further in view of Chang, and claims 39-41 under 35 U.S.C 103(a) as being obvious over Grisamore in view of Greenburger, in further view of Chang, in further view of Fang. Beginning with claim 32, the Examiner already concedes that Grisamore is lacking one or more elements of the rejected claims. For example, the Examiner states: "Grisamore does not implicitly disclose two paths one for a real component branch, inverting certain partial produces and passing the inverted and non-inverted partial products and one for an imaginary component branch, passing the partial products to a multi-stage series of Boolean function generators simultaneously." It is respectfully submitted that even if the successful combination of Grisamore with Greenburger, and/or Chang and/or Fang were made, although, as stated previously, Assignee has serious doubts concerning the ability to do so, the resultant combination or any of the other alleged combinations would still not recite the elements of the rejected claims. Greenburger is directed toward a complex number multiplier circuit, and does not provide the deficiencies of Grisamore and/or Chang and/or Fang, noted above. For example, neither Grisamore, Chang, Fang nor Greenburger recite simultaneously passing the partial products from the two or more input terms to a multi-stage series of Boolean function generators that implements one or more full-adders and associated registers, half-adders and associated registers, and single registers to produce intermediate summation results by combining the partial products.

It is respectfully submitted, therefore, that at least one element of claim 32 is absent from the cited art, and any alleged combination would still not result in a combination having each element of the rejected claim. Therefore, a prima facie case of obviousness under section 103 of the patent statute has not been made. It is, therefore, respectfully submitted that claim 32 is in condition for allowance.

Claims 33-43 depend from and include all limitations of claim 32, and distinguish from the cited art at least on the same basis as claim 32. It is therefore respectfully requested that the Examiner withdraw his rejection of these claims.

Attorney Docket: 012.P10008

CONCLUSION

In view of the foregoing, it is respectfully submitted that all claims presented are in a condition for allowance, and early allowance of all claims pending in the application is respectfully requested. If the Examiner has any questions, he is invited to contact the undersigned at (503) 439-6500.

Please charge any shortages and credit any overcharges of any fees required for this submission to Deposit Account number 50-3703.

Respectfully submitted,

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